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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,113	10/11/2001	Clifford R. Johns	LUT 2 0059	8775

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EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 09/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,113	JOHNS ET AL.	
	Examiner	Art Unit	
	Tuan A Vu	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed October 11, 2001.

Claims 1-15 have been submitted for examination.

Claims objections

2. Claim 10 is objected to because of the following informalities: there recited group 'compiler selective converting the input file (line 5 of claim 10) appears to have 'selective' as a misplaced or mistyped element. Examiner will interpret this group element as 'compiler operative for selectively converting' to examine the merits of the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Schaumont et al., USPN: 6,606,588 (hereinafter Schaumont).

As per claim 1, Schaumont discloses a method of designing hardware, comprising:

entering source code into source code file, said source code a context-free grammar that describes a job the hardware being designed has to do (e.g. Vector model *307*, Data-flow model *315* – Fig. 3; *behavioral description*, col. 3, lines 20-31; Figs. 6-10; col. 51, line 19 to col. 60,

line 14; col. 65, lines 31-42; Fig. 21; *metacode generation* - col. 4, line 2 to col. 49, line 43 – Note: Vector modeling with rules firing upon input/output mapping and meta code describing SFG type graph based on input/token mapping according to a finite state machine are equivalent to context free grammar embodied as source file stored in Matlab model library – see col. 8, lines 2-4) rather than describing an implementation of the hardware; and

compiling the source code file to generate an output file which describes an optimized state machine for implementing the hardware (e.g. code 306 – Fig. 3; col. 75-226; *C++ code generation* – Fig. 22 – Note: simulation, scheduling, profiling and bench-marking amounts to generating *optimized* state machine responses – see col. 8, lines 32-44; cols. 17-36), said output file being written in C-based code.

As per claim 2, Schaumont discloses output file describing transmit and receive state machines (e.g. *sfg1, sfg2, sfg3, sfg/fsm* - Fig. 7; FSM, component 1, FSM component 2 – Fig. 21 – Note: FSMs firing from rules after receiving some input is equivalent to transmit and receive state machine associated with C++ code generated).

As per claim 3, Schaumont discloses HDL and RTL (e.g. Descriptions *2206, 2208* -Fig. 22).

As per claim 4, Schaumont discloses, based on the SFG of source code:

identifying sequences of states (e.g. col. 195, lines 293-310; col. 97 lines 63 to col. 105, line 390 – Note: collapsing state sequences, i.e. array element value, under one state dictated by a conditional or logical expression is equivalent to collapsing sequences under one state) in the source code occurring more than twice in a row (*loop_cycle[ ]* -col. 195 line 299);

collapsing the sequence into one state (e.g *phi <= NCYC*, col. 195, line 306; *i=0; i<NF+F*, line 344 – Note: bounding all sequence of states being defined under one fsm controller control statement is equivalent to collapsing states into one condition whose state is determined from that that conditional statement); and

wrapping a counter around that one state (*int phi <= NCYC*, col. 195, line 298; *i=0; i<NF*, line 335).

As per claim 5, Schaumont describes FSM and firing rules according to some data graph and vector, hence implicitly disclose grammar free context, hence inherently teaches Backus Naur Formalism.

As per claim 6, Schaumont discloses a computer-readable medium embodying a computer software for designing hardware, comprising:

a compiler which generates from source code an output file that describes an optimized state machine for implementing hardware (e.g. code 306 – Fig. 3; col. 75-226; *C++ code generation* – Fig. 22 – Note: simulation, scheduling, profiling and bench-marking amounts to generating optimized code – see cols. 17-36; col. 8, lines 32-44);

said source code using a context-free grammar that describes a job the hardware being designed has to do (e.g. Vector model *307*, Data-flow model *315* – Fig. 3; *behavioral description*, col. 3, lines 20-31; Figs. 6-10; col. 51, line 19 to col. 60, line 14; col. 65, lines 31-42; Fig. 21; *metacode generation* - col. 4, line 2 to col. 49, line 43); and

said output file being written in a C-based language (*C++*, code *306* – Fig. 3).

As per claim 7, refer to rejection of claim 2.

As per claim 8, this claim corresponds to claim 4 above, and is rejected using the corresponding rejection as set forth therein.

As per claim 9, Schaumont discloses an user option that puts variables in the output file which have names matching those corresponding to source code node (e.g. col. 22, line 49 to col. 32, line 6), said variables getting set of defined value in every state generated from its corresponding node (e.g. col. 32, line 54 to col. 36, line 61 – Note: populating variables declared from the SFG nodes and providing for each variables being declared a value corresponding with a state analysis from the SFG simulation process reads on matching variables corresponding to source code node and variables getting set of defined value in every state generated from SFG source model; col. 129, lines 230-267; col. 195, lines 323-350– Note: for each *maps[]* or *I_sample[]* or *Fq_coef[]* element of a SFG a value is set)

As per clam 10, Schaumont discloses a system for designing hardware, said system comprising

computer means for entering an input file written in a source code using a context-free grammar which describes a job the hardware being designed has to do (e.g. Vector model *307*, Data-flow model *315* – Fig. 3; *behavioral description*, col. 3, lines 20-31; Figs. 6-10; col. 51, line 19 to col. 60, line 14; col. 65, lines 31-42; Fig. 21; *metacode generation* - col. 4, line 2 to col. 49, line 43);

a computer compiler operative for selectively converting the input file into an output which is written in a C-based code, said output file describing an optimized state machine for implementing the hardware being designed (e.g. code 306 – Fig. 3; col. 75-226; *C++ code generation* – Fig. 22 – Note: simulation, scheduling, profiling and bench-marking amounts to

generating optimized code – see cols. 17-36; col. 8, lines 32-44-- and scheduling in support of profiling implicitly disclose a selection of functions based on time efficiency observing rules or profile data).

As per claim 11, Schaumont discloses C-based code translated to HDL (e.g. Descriptions *2206, 2208* -Fig. 22).

As per claim 12, refer to claim 3 and col. 4, lines 25-37.

As per claim 13, Schaumont discloses selectively generating output files which describe both transmit and receive state machines (e.g. *sfg1, sfg2, sfg3, sfg/fsm* - Fig. 7; FSM, component 1, FSM component 2 – Fig. 21 – Note: base on token and rules of the associated FSM and SFG for generating the C++ code is equivalent to selectively yielding results for implementing in code statements).

As per claim 14, this claim corresponds to claim 4 above, and is rejected using the corresponding rejection as set forth therein

As per claim 15, refer to claim 5.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or: (703) 746-8734 (for informal or draft communications, please label "PROPOSED" or "DRAFT" – please consult Examiner before use)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA. , 22202. 4th Floor(Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

VAT
September 6, 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
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